IN THE CLAIMS

Claims 1-14 (Canceled).

15 (Currently Amended). A method for mounting multiple semiconductor dies on a single leadframe having fingers, comprising:

stacking at least two semiconductor dies having substantially the same rectangular dimensions on top of one another such that one of said dies is mounted on top of the leadframe fingers and the other of said dies is mounted on and in contact with the die mounted on the leadframe fingers; and

wirebonding each of said semiconductor dies to the same leadframe fingers.

16 (Previously Presented). The method of claim 15, wherein one of said semiconductor dies is mounted back to back on the other of said semiconductor dies.

17 (Previously Presented). The method of claim 16, wherein one of said semiconductor dies is adhered to the other of semiconductor dies by an adhesive layer.

18 (Original). The method of claim 15, wherein a first semiconductor die has a lead-on-chip configuration.

19 (Original). The method of claim 15, wherein one of said dies is secured to said leadframe and the other of said dies is secured to the die secured to the leadframe.

20 (Original). The method of claim 15, further comprising wirebonding the semiconductor dies to the leadframe, said dies having facing sides and outwardly facing sides by extending wires to bond pads on the outwardly facing sides of said die.

21 (Currently Amended). A method of connecting multiple semiconductor dies having bonding pads and a single leadframe having lead fingers, comprising:

locating a first semiconductor die on the lead fingers of the leadframe;

stacking a second semiconductor die on said first semiconductor die and in contact with said first semiconductor die; and

electrically connecting the bonding pads of the semiconductor dies to the same lead fingers of the leadframe.

22 (Original). The method of claim 21, further comprising encapsulating the semiconductor dies and the leadframe in a single package body.

Claims 23-31 (Canceled).

32 (Currently Amended). A method for mounting multiple semiconductor dies on a single leadframe having fingers, comprising:

stacking first and second semiconductor dies having substantially the same rectangular dimensions on top of and in contact with one another;

mounting the first semiconductor die on a leadframe finger;

mounting the second semiconductor die ~~only~~ on said first semiconductor die; and

wirebonding the first and second semiconductor dies ~~electrically connecting bonding pads on each of said semiconductor dice~~ to the same lead fingers of the leadframe.

Claim 33 (Canceled).

34 (Previously Presented). The method of claim 32 wherein the first semiconductor die is mounted back to back on the second semiconductor die.

35 (Previously Presented). The method of claim 34 wherein the first semiconductor die is adhered to the second semiconductor die by an adhesive layer.

REMARKS

As now amended, claims 15 and 21 distinguish over Sota.

With respect to claim 33, it is respectfully submitted that the asserted rationale to combine is not from within the prior art, but is only the result of the benefit of hindsight reasoning. Absent a rationale to combine from within the prior art itself, no *prima facie* of Section 103 rejection is made out. Here, since the Section 103 rejection is based on a single reference which admittedly fails to teach all the elements, a *prima facie* rejection is not made out.

In view of these remarks, reconsideration of the application is respectfully requested.

Respectfully submitted,

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